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AN 8-BIT PIPELINE ADC IN 65NM WITH 250MHZ NYQUIST FREQUENCY TO OBTAIN 6B ENOB

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ABSTRACT

In this paper, an 8-bit Pipeline ADC, with 1V supply at 250MHz Nyquist frequency has been proposed. The ADC architecture uses 1.5bit stages as sub-ADCs for power reduction. This work targets 6b ENOB at both low and high input frequencies (ranging from 1-7MHz). The design has been implemented in 65nm CMOS technology. Comparative power consumption for 180nm, 90nm and 65nm is obtained which shows a reasonable power reduction of 3.067mW from 180nm to 65nm.

KEYWORDS: Analog-to-Digital Converter (ADC), Interleaved Sample and Hold Circuit (ISHC), Multiplying DAC (MDAC), high speed, low power.

1. Introduction

In today's date in industries, data acquisition, industrial measurement and communication are the most vogue applications. This can be smoothly accomplished using mixed signal integrated circuits. Mixed signal IC consists of analog and digital circuits on the same semiconductor die. ADC and DAC are the link between analog transducers and digital world of signal processing and data handling [1]. And thus ADC holds great importance for providing cost-effective solutions for building any modern consumer electronics applications. Due to the increasing demand of high speed and low power applications, the nature of corresponding ADCs also need to be optimized.

The proposed ADC here uses interleaved sampling which helps in achieving higher speed. Instead of using interleaving scheme for the overall structure, it uses interleaved building blocks. The individual stage itself is a pipeline ADC. This results in a lower aggregate input capacitance, which helps in overall power reduction. [2]

In Section II, ADC architecture is explained in detail. Section III explains the internal components of each stage like Interleaved Sample & Hold Circuit (ISHC), Comparator & Multiplying Digital to Analog Converter (MDAC). In Section IV, layout vs schematic characteristics are shown. The experimental results are represented in Section V and finally in Section VI paper is concluded.

2. ADC Architecture

As shown in fig.1, this ADC architecture has 8 blocks which comprises of a Track & Hold stage (T&H), 6 1.5 bit stages and a 2 bit Flash ADC. The outputs of all the 1.5bit stages and 2bit Flash are given to the digital calibration block. Digital calibration can be performed on-chip by internal gain correction or off chip using appropriate correction algorithm. Here, internal gain correction is used to minimize the errors.

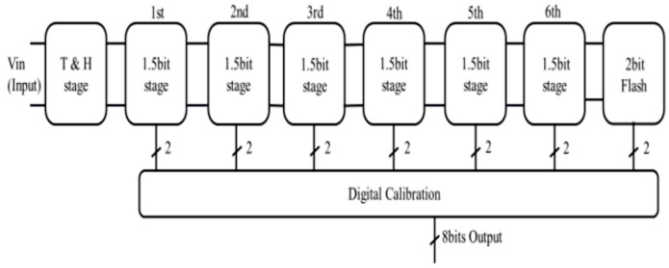


Figure.1 Architecture of 8bit Pipeline ADC

2.1 Interleaved Sample & Hold Circuit

Each pipeline stage needs to process the data in one clock cycle itself. In this process MDAC takes an entire clock period for settling [2].Hence, interleaved sampling is used. From fig. 3, this stage uses 4 nMOS switches and 2 current mode buffers.

Current mode buffer serves 2 purposes: a) Prevention of charge sharing between sampling capacitor and input capacitance of MDAC and b) Convert nMOS signal level at input to a pMOS signal level at the output. [3]

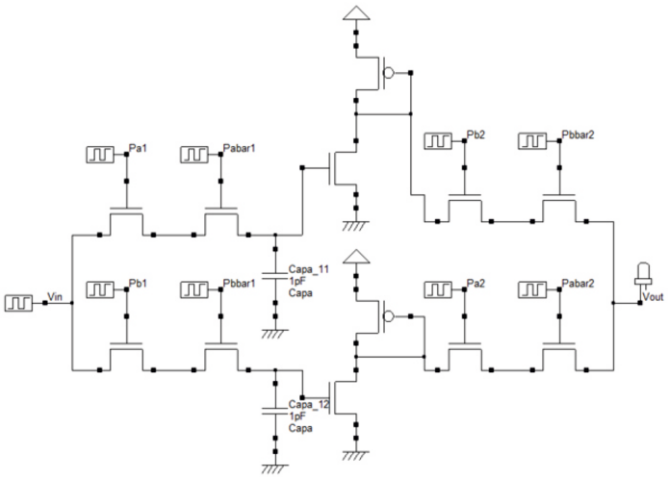
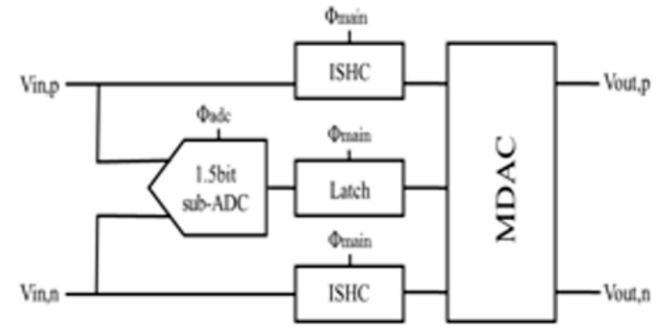


Figure.2 Double sampling circuit

2.2 Sub-ADC (1.5bit stage)

As stated before, each sub-ADC here is an individual 1.5bit pipeline ADC. As shown in fig.3, it consists of a comparator, latch and MDAC.



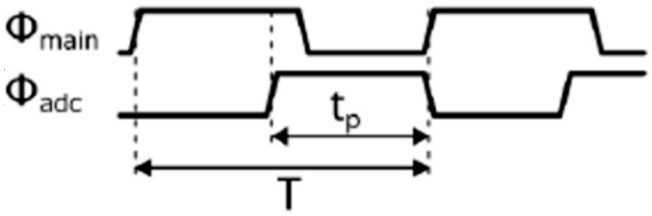


Figure.3 a) 1.5bit stage b) Use of non-overlapping clocks to enable coarse ADC to operate during non-overlapping time

A 1.5-bit stage is actually a 1-bit stage which has some inbuilt redundancy to provide a large tolerance for component variations, imperfections and tolerances. A digital calibration algorithm later eliminates the redundancy. A 1.5-bit stage in fact represents approximately 1.5 bits. Two symmetrical analog comparison levels, VH and VL are present, instead of one. The amplifier has a gain of 2. VH and VL must lie between the range of -VR/2 and +VR/2. [1]The main reason behind using minimum stage resolution of 1.5bit instead of the more common 3bits is that it minimizes the required inter-stage gain and maximizes the bandwidth along with small die area. [4]

A) Comparator

Figure.4 shows the comparator used in sub-ADC. A differential pair comparator based on Strong ARM sense amplifier latch is used.

The use of differential configuration helps in reducing mismatch-induced offset and optimizing the speed. The standard deviation of the offset can be lowered by increased device sizes and proper layout. [6] Clocked latches are used after the comparator. The digital outputs need to be available at the beginning of the next clock period, hence no additional time is given to the latches to suppress metastability. [2]

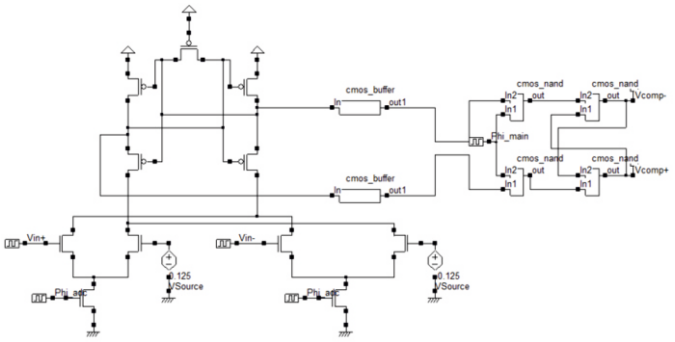


Figure.4 Differential pair comparator with StrongARM sense amplifier latch

B) Multiplying DAC(MDAC)

Due to the advantage of variable reference voltage MDAC is an ideal choice for the pipeline ADC. A differential input signal Vin, p = VCM+ΔV, Vin, n = VCM-ΔV, is used at pMOS levels, to drive a p-to-n-stage, where the pMOS levels are converted to nMOS levels, making both available. In the next stage, M3p adds a current from Vin, p to the output node and M5p subtracts a current from Vin, n from the same node. Hence we create Vin,p-Vin,n = 2ΔV, the input signal doubled with common-mode removed.

M4p and M6p act as DAC by adding or subtracting an appropriate current to the output node. Use of both nMOS and pMOS DAC transistors enable a differential voltage to be both added and subtracted to the output while leaving the CM level unchanged. M7p is used to set the output CM level and M8p finally forms the load of this stage, thus creating an output voltage with nMOS levels. Usually, the gain of the different stages differs from their nominal value due to nonzero output conductance of the transistors (gd0≠0). Therefore all gains are adjusted by varying the transistor widths.

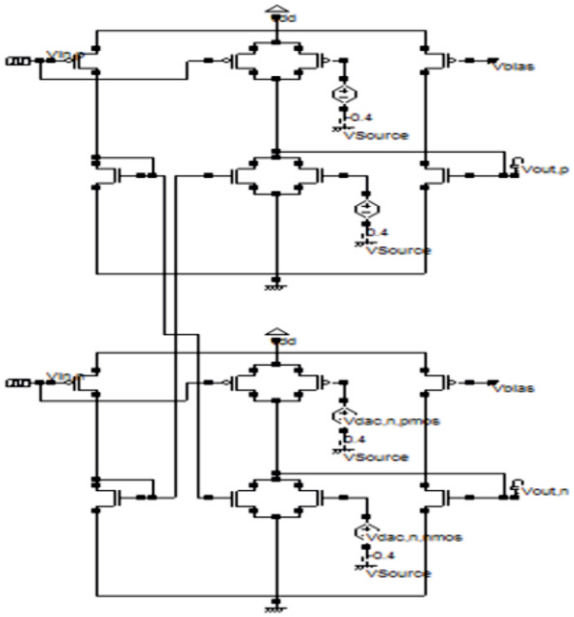


Figure.5 MDAC circuit

3. Experimental Results

3.1 Layout vs Schematic

Schematic simulations are often smooth but when the circuit is implemented in form of layout, several issues come up. Like delay errors, design rule errors, complex routing and the challenge of area minimization.[5]

Hence, in this section basic building blocks of the architecture are implemented in layout using Microwind 3.5 and characteristic results are obtained.[7]

A) Interleaved S&H Circuit(ISHC)

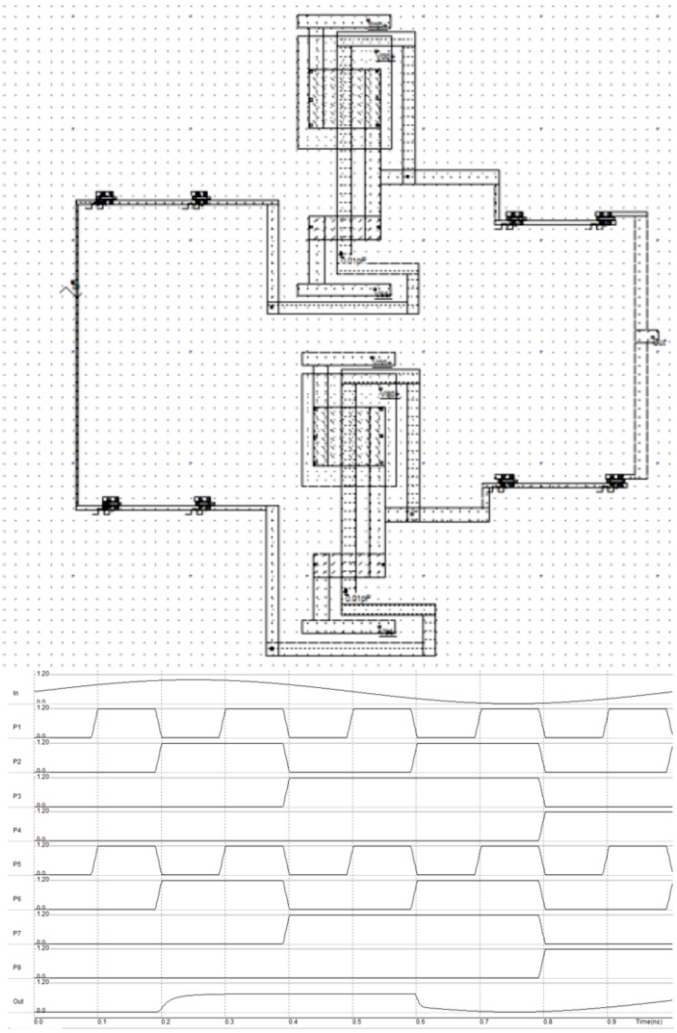
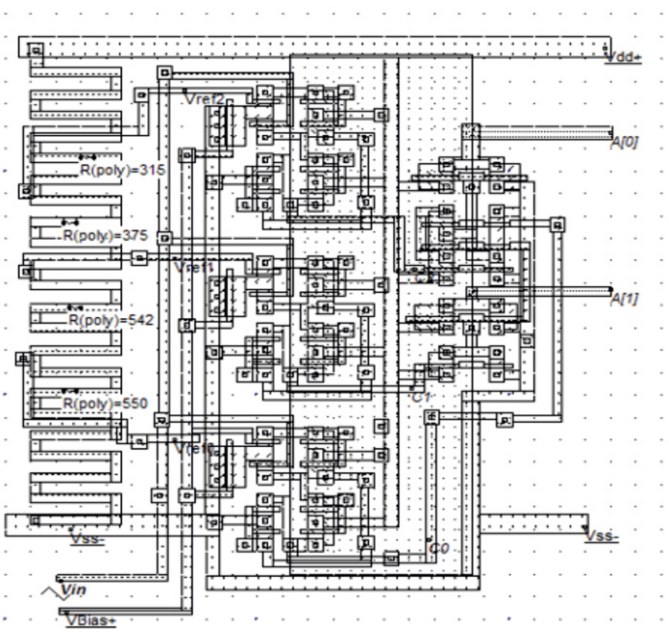


Figure.6 a)ISHC layout b)Output

B) 2bit Flash ADC



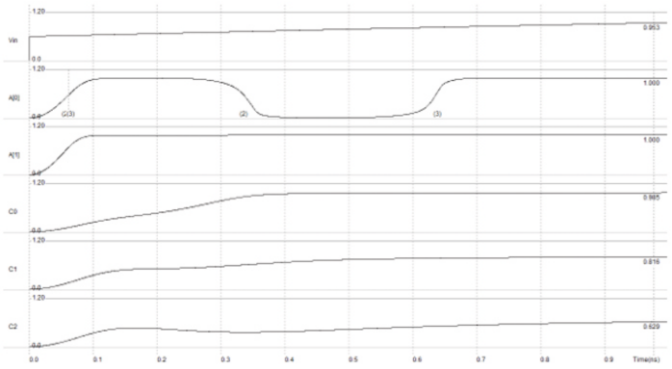
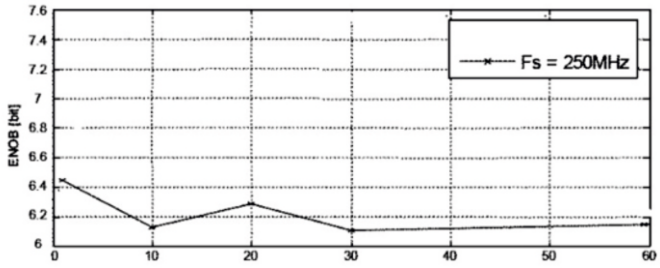


Figure.7 a)2 bit Flash ADC layout b)Output

3.2 Performance parameters

Three parameters are obtained for the proposed pipeline ADC. At fs=250MHZ, 6bits ENOB is obtained instead of the ideal 8bits resolution.



DNL and INL errors are also measured which are obtained +1.2/-0.9 LSB and +1.2/-1.4LSB respectively.

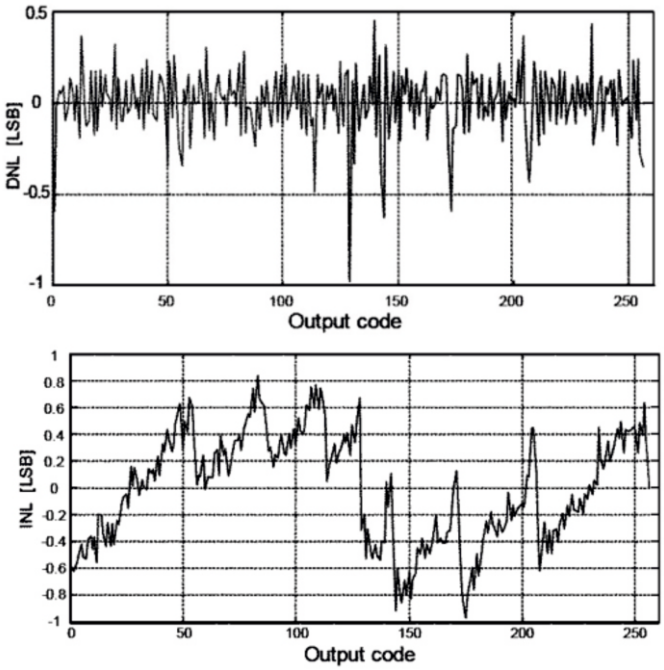


Table.1 Perfomance of the proposed ADC

Technology	65nm
Sampling rate	250MS/s
ENOB	6bits
DNL	+1.2/-0.9LSB
INL	+1.2/-1.4 LSB

Table.2 Comparison

Technology	Power
180nm	3.526mW
90nm	0.955mW
65nm	0.459mW

IV Conclusion

This pipeline ADC uses the 1.5bit sub-ADCs with interleaved sampling.Thus enabling it to achieve higher speed of 250MS/s. The internal gain calibration in MDAC minizes DNL and INL errors to +1.2/-0.9LSB and respectively. Power consumption measured shows that when the proposed ADC is scaled down to 65nm the power reduces to 0.459mW, thus a reduction of 3.067mW is obtained from180nm to 65nm.

Acknowledgement

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